

**Remarks**

Claims 1-8 are pending in the present application.

The specification has been amended to properly identify the issued patent number according to US practice.

**35 U.S.C. § 112, second paragraph Rejection**

Claims 1-4 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. These claims have been reviewed and revised to clarify the invention in accordance with the Examiner's suggestions. In view of the absence of any prior art rejection of these claims, these claims are deemed allowable and indication of such allowance of claims 1-4 is deemed proper and respectfully requested.

**35 U.S.C. § 102(b) Rejection**

Claims 5-8 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Kishi (U.S. Patent No. 5,985,722). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

Regarding independent claim 5, the Examiner equates Kishi's three field oxide films 2, 2, 2 shown in Figure 3 to Applicant's first, second and third device isolation layers. The Examiner also equates Kishi's gate electrodes 5A and 5B to Applicant's gate electrode. According to this reading, however, Kishi's gate electrode having a polysilicon layer is not formed "on the first device isolation layer" as required by claim 5, since the gate electrodes 5A, 5B are formed

between Kishi's field oxide films 2, 2 and not on one of these oxide films. In clear contrast, in Applicant's embodied invention as shown in Figure 5, the gate electrode 85 having the polysilicon layer 69 is formed on the device isolation layer 62. Thus, this feature as recited in claim 5 is completely absent from Kishi.

In addition or in the alternative, the Examiner equates Applicant's metal line layer of claim 5 to Kishi's silicide layers 13A, 13B, 14A, 14B and Applicant's input pad layer to Kishi's electrode 15C. However, only Kishi's silicide layer 13A is formed underneath Kishi's electrode (input pad layer) 15C, but Kishi's silicide layer 13A does not selectively and electrically connect the electrode 15C to either the polysilicon layer (Kishi's 5B) or a ground source. In Kishi, the silicide layer 13A is electrically isolated from the gate electrode 5B by the insulating layers 10, 12 and 4.

Therefore, Kishi fails to anticipate, *inter alia*:

forming a gate electrode having a polysilicon on the first device isolation layer;...

forming a metal line layer underneath the input pad layer for selectively and electrically connecting the input pad layer to either the polysilicon layer or a ground source

as recited in independent claim 5.

Accordingly, claim 5 and their dependent claims (due to their dependency) are allowable over the applied reference, and the rejection should be withdrawn.

### **Conclusion**

For the foregoing reasons and in view of the above clarifying amendments, Applicant respectfully requests the Examiner to reconsider and

withdraw all of the objections and rejections of record, and earnestly solicits an early issuance of a Notice of Allowance.

Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Esther H. Chong (Registration No. 40,953) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Applicant(s) respectfully petitions under the provisions of 37 C.F.R. § 1.136(a) and 1.17 for a one-month extension of time in which to respond to the Examiner's Office Action. The Extension of Time Fee in the amount of \$120.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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